[0155] When the SiN_z film having the semiconducting property is manufactured under the aforementioned conditions and an additional condition that the thickness of the film is to be 16 nm, a current density of 2.5×10^3 A/cm^2 is obtained by the application of a voltage of 1.6 V and a current density of 5×10^2 A/cm^2 is obtained by the application of a voltage of 0.8 V. Thus, when these voltages are used as the standards, an On/Off ratio is 5. The non-ohmic element having such a configuration can be adequately used as the non-ohmic element included in the non-volatile semiconductor memory element.

[0156] Although the connection electrode **73** is provided on the lower electrode surface of the variable resistance layer **76** in Embodiment 4, this is not necessarily essential. For example, depending on the material selected for the variable resistance layer **76**, the connection electrode **73** is unnecessary. In this case, the non-volatile semiconductor memory device may have the same configuration as the non-volatile semiconductor memory device **10** in Embodiment 1.

Embodiment 5

[0157] The following is a description of Embodiment 5 according to the present invention, with reference to FIG. **18**.

[0158] FIG. **18** is a diagram showing configurations of a variable resistance element **103** and a non-ohmic element **106** which are essential parts of a non-volatile semiconductor memory device in Embodiment 5 according to the present invention. More specifically, in FIG. **18**, (a) shows a top view and (b) shows a cross-section diagram viewed in the direction of arrows along a line **6A-6A** shown in (a).

[0159] The non-volatile semiconductor memory device in Embodiment 5 has the same basic configuration as the non-volatile semiconductor memory device **10** in Embodiment 2, and is different from the non-volatile semiconductor memory device **10** in that a semiconductor layer **107** and an upper electrode **108** included in a non-ohmic element **106** are formed separately for each of variable resistance elements **103**.

[0160] To be more specific, in the non-volatile semiconductor memory device shown in (b) of FIG. **18**, a variable resistance layer **104** and a shared electrode **105** are formed in a memory cell hole formed in an interlayer insulating layer **102** on a lower electrode line **101**, and the semiconductor layer **107** and the upper electrode **108** are formed on the shared electrode **105**. As a result, the non-ohmic element **106** including the shared electrode **105**, the semiconductor layer **107**, and the upper electrode **108** is formed.

[0161] Then, an upper line **110** is formed on the interlayer insulating layer **109** in which the non-ohmic element **106** is filled and on the upper electrode **108**. A plurality of upper lines **110** are formed in parallel, extending in a second direction intersecting with (for example, orthogonal to) a first direction in which the lower electrode line **101** extends. The upper line **110** is formed by patterning, after a conductive material layer is formed on the interlayer insulating layer **109** and the upper electrode **108**. Here, the conductive material layer comprises, for example, aluminium (Al) or copper (Cu) commonly used as an electrode material in the semiconductor process.

[0162] With this configuration, the semiconductor layer **107** and the upper electrode **108** of the non-ohmic element **106** can be provided independently for each of the non-ohmic elements **106**. Thus, an optimum material can be selected for each of the semiconductor layer **107** and the upper electrode **108** of the non-ohmic element **106**. Moreover, the upper layer line **110** is formed directly on the upper electrode **18**. This can simplify the process of connecting the upper layer line **110** to an active element (not illustrated) via a buried conductor (not illustrated, but corresponding to the buried conductor **28** shown in (b) of FIG. **6** for example) in a contact hole provided outside the matrix region (where the memory cells, each of which includes the variable resistance element **103** and the non-ohmic element **106**, are arranged in the array). To be more specific, the process of eliminating the semiconductor layer of the non-ohmic element in the contact region can be omitted. Thus, the dual damascene method can be used, thereby simplifying the process.

[0163] As in the case of the non-volatile semiconductor memory device in Embodiment 3, each of the non-volatile semiconductor memory devices in Embodiments 4 and 5 may have the stacked structure including a plurality of memory cell arrays.

[0164] Moreover, in Embodiment 5, one non-volatile semiconductor memory element includes one non-ohmic element and one variable resistance element. However, the present invention is not limited to this. For example, a plurality of non-ohmic elements may be separated at one time, instead of one at a time.

[0165] Embodiments have been described thus far. In each of Embodiments described above, the variable resistance layer is all filled inside the memory cell hole. However, by forming the first variable resistance layer **212***a* on a front layer part of the lower electrode line, the first variable resistance layer **212***a* may be positioned outside the memory cell hole.

[0166] Each of Embodiments describes the case, as an example, where a tantalum oxide is used for the variable resistance layer. However, a hafnium oxide may be used instead of the tantalum oxide. By performing the plasma nitriding process on the hafnium oxide, a hafnium nitride is formed. Here, the hafnium nitride has conductivity (for example, 225 μΩcm of substrate-temperature resistivity). On account of this, the hafnium nitride can be easily used for the variable resistance layer according to the present invention in which the plasma nitriding process is performed on the hafnium oxide to form the shared electrode.

[0167] Moreover, it is preferable for the first electrode **201** coming contact with the first variable resistance layer **212***a* to comprise one or more of materials having higher standard electrode potentials than tantalum or hafnium used as the transition metal included in the variable resistance layer. Such materials include Au (gold), Pt (platinum), Ir (iridium), Pd (palladium), Ag (silver), and Rh (rhodium). With this configuration, a resistance change operation can be stably caused in the variable resistance layer.

[0168] Furthermore, each of Embodiments above describes the case where the MSM diode is used as an example of the non-ohmic element. However, an MIM diode or a varistor may be used instead of the MSM diode. To be more specific, even when the semiconductor layer of the MSM diode is replaced by an insulator layer or a semiconductor ceramic layer, the same advantageous effects as in Embodiments above can be obtained.

[0169] It is to, be noted that, from the above description, various changes and modifications are apparent to those skilled in the art. Therefore, the embodiments disclosed thus far only describe examples in all respects and are intended only to show, to those skilled in the art, examples of aspects